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OPTIMAL LAYOUT OF CMOS FUNCTIONAL ARRAYS.(U)
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T. Uehara
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Technical Report No. 142

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This work was supported by the Joint Services Electronics Program under contract N-00014-75-C-0601.

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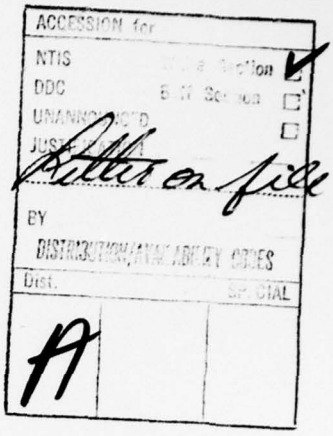
Optimal Layout of CMOS Functional Arrays



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ABSTRACT

Designers of MOS LSI circuits can take advantage of complex functional cells in order to achieve better performance. This paper discusses the implemention of a random logic function on an array of CMOS transistors. A graph-theoretical algorithm which minimizes the size of an array is presented. This method is useful for the design of cells used in conventional design automation systems.

INDEX TERMS: CMOS functional arrays, CMOS circuit design, LSI layout, LSI design automation, computer-aided design, design automation

1. INTRODUCTION

In integrated circuit design it is possible to implement a logic function by means of a circuit consisting of one or more elementary cells such as NAND or NOR gates or by means of a single functional cell.

The basic advantages of functional cells, such as smaller size and better performance, are well known to designers of MOS LSI [1]. Theoretical results about network synthesis with complex functional cells have been reported in [2], [3], [4]. Some commercial products also take advantage of these properties [5]. However, most designers still use a limited library of cells. For example, NAND gates are often used as the only primitive cell. This is partly due to the fact that little has been reported about the physical implementation of complex functional cells [6]. Therefore, designers do not have confidence in the performance and merit of more complex cells. In order to overcome these problems, a systematic enumeration of functional cells is inevitable.

The number of useful functional cells is enumerated in this paper. This number is so large that a systematic layout method is necessary. An array of CMOS FET's is introduced as the basic layout and a graph- theoretical algorithm which minimizes the size

of the array is presented. This type of array is also useful as a basic cell for conventional design automation systems [7], [8] because it has a rectangular shape with the same height as the other cells. Several examples show the significant merit of functional cells in reducing the space required.

2. CMOS FUNCTIONAL CELLS

An implementation of the exclusive-or funtion $\bar{X}Y + X\bar{Y}$ is shown in Figure 1, where the designer was required to use NAND gates throughout. An alternative implementation of the same function is shown in Figure 2 [1], where the designer took advantage of the functional cell which realizes the function $\overline{XY + \bar{Z}}$. This approach results in better performance and smaller size than the design of Figure 1.

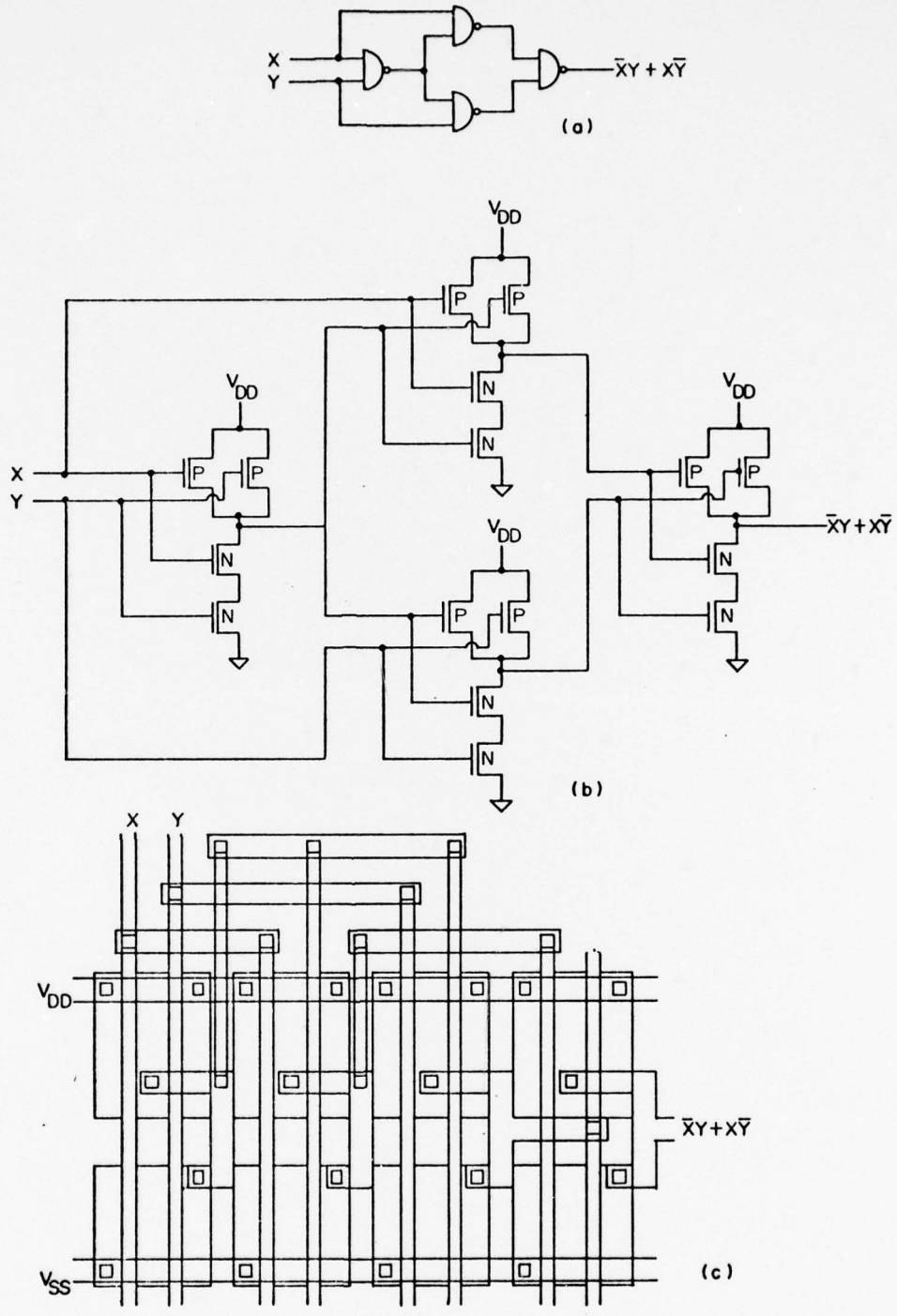


Figure 1: Implementation of an exclusive-or function.
a) logic diagram b) circuit c) layout

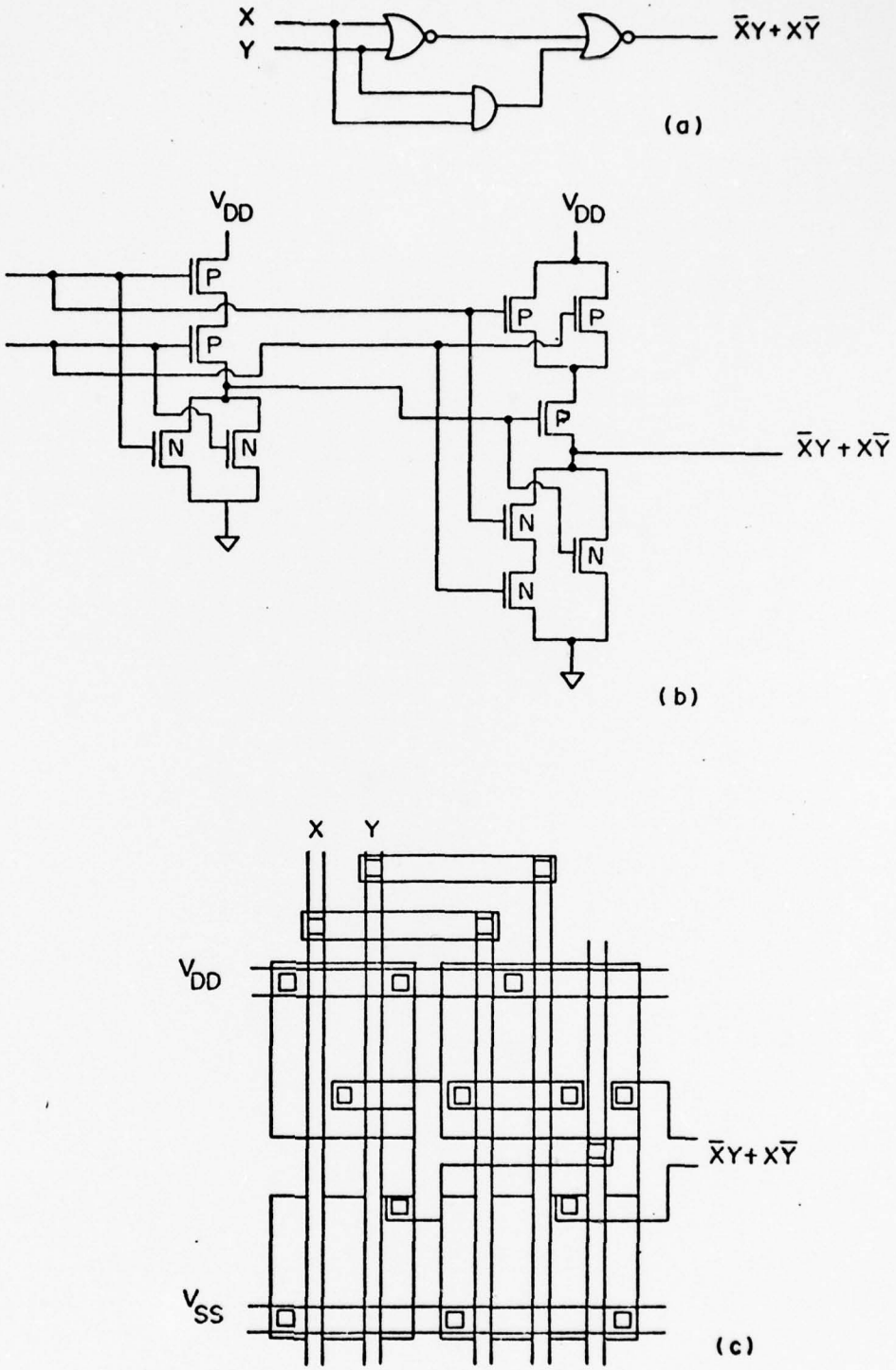


Figure 2: An alternative implementation of the exclusive-or function.
a) logic diagram b) circuit c) layout

3. ENUMERATION

In this paper, we will limit ourselves to AND-OR networks realized in CMOS by means of series/parallel connections of transistors. Furthermore, we will require that the topology of the p-MOS and n-MOS sides of the circuit are each other's dual.

The number of functional cells which has series/parallel topology is shown in Table 1, where the maximum number of series FET's between the power and the output is designated as the level of a cell. The details of the enumeration are shown in the Appendix.

Number of levels	Number of cells
1	1
2	6
3	80
4	3434

Table 1: Number of cells with a given level.

The delay of a cell mainly depends on the number of levels since it corresponds to the longest path to charge the capacitance. Generally, cells with less than 4 levels are desirable. To use all of the cells with 3 levels and some with 4 levels seems to be a reasonable compromise, although the decision about the usefulness of cells is beyond the scope of this paper. In any case, systematic design is inevitable in order to treat more than several hundred cell types.

4. BASIC LAYOUT STRATEGY

The basic layout scheme for an arbitrary logic function is given in this section, starting from the corresponding AND/OR (sum of products) specification.

A cell is an array of CMOS transistors as shown in Figure 3. It consists of a row of p-MOS transistors and a row of n-MOS transistors corresponding to the p-MOS and n-MOS sides of the circuit, respectively. Because of the requirement that the p-MOS and n-MOS sides are each other's dual, the number of transistors is the same in both rows. We will further assume that the transistors are aligned vertically. AND/OR gates in the logic diagram correspond to the series/parallel connections in the circuit diagram. It is quite clear that for every AND/OR specification of a boolean function, one can obtain a series-parallel implementation in CMOS technology, in which the p-MOS side and n-MOS sides are each others dual. The number of series/parallel transistors for every AND/OR element is equal to the number of inputs to that element. The dual topology of the p-MOS side and of the n-MOS side are as shown in Figure 3(c).

A more general topology other than series/parallel can be used in a MOS circuit as in the case of a relay network. The

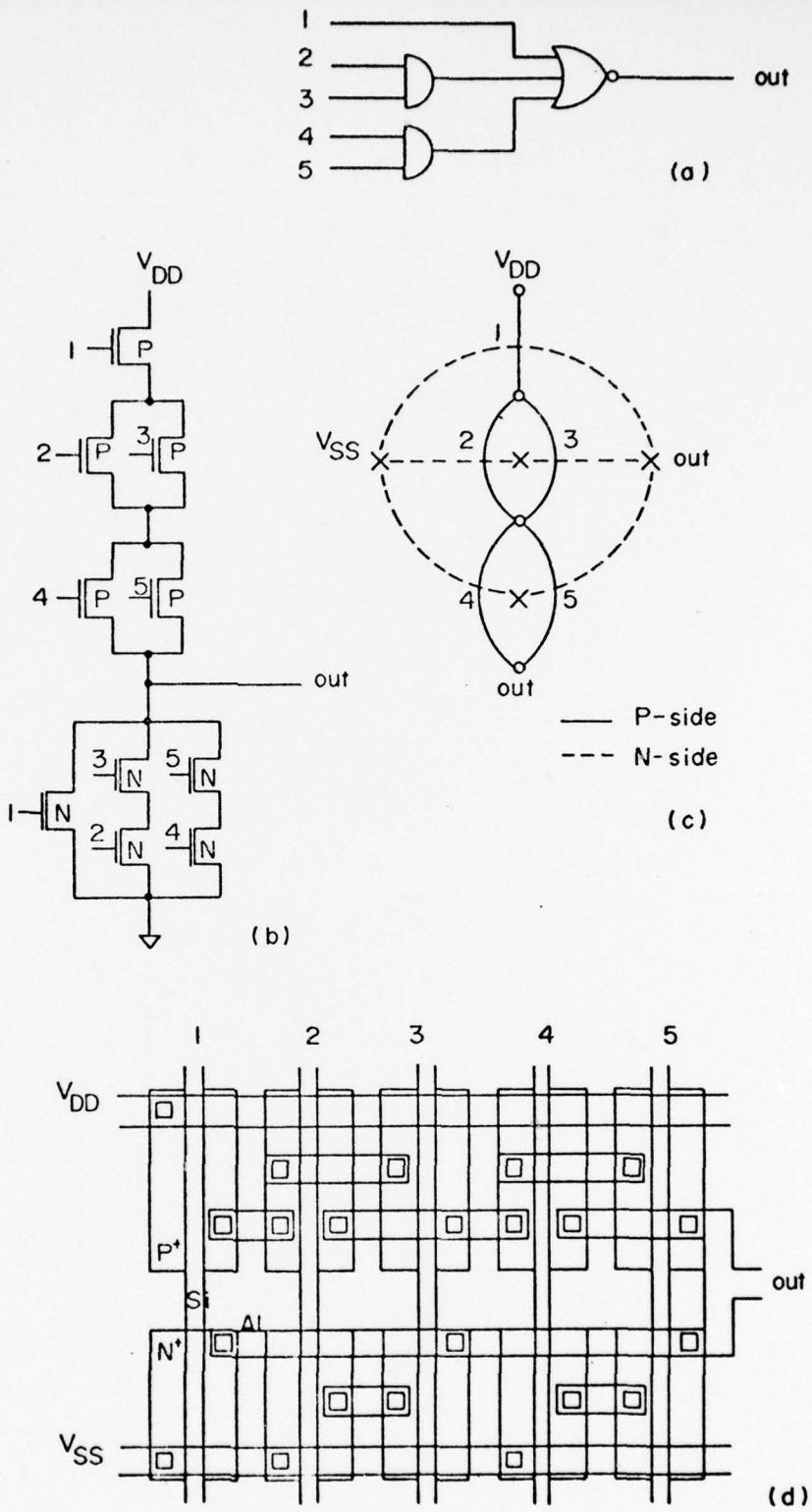


Figure 3: Basic layout of the functional cell.
a) logic diagram b) circuit c) graph model d) layout

topology of the p-MOS side and the n-MOS side need not to be dual in the strict sense. However, the series-parallel connection and the duality are assumed here in order to simplify the problem.

5. OPTIMAL LAYOUT

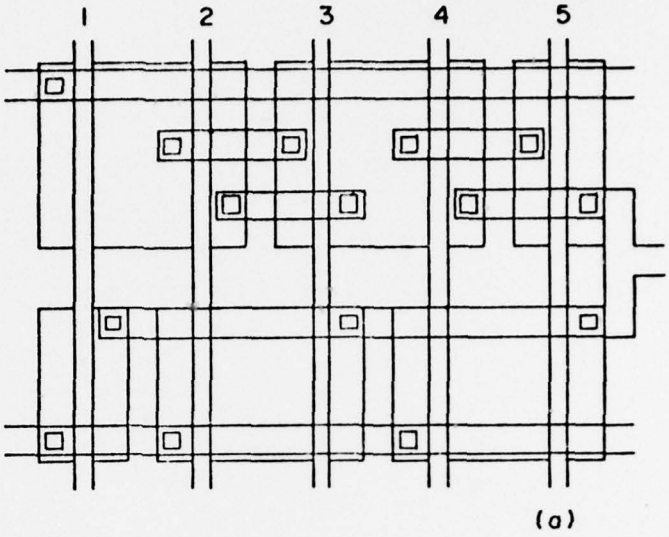
A graph theoretical algorithm for minimizing the size of a functional array is developed in this section.

5.1 Preliminary Considerations

Physically adjacent gates can be connected by a diffusion area. The aluminium connections between neighbors, as in Figure 3(d), are replaced by diffusion areas as shown in Figure 4(a), but the size of the array was not changed. Even in a more sophisticated layout arrangement, the alignment between p-MOS side and n-MOS side is required. Figure 4(b) is a more optimal size layout for the circuit of Figure 3(b).

However the best result is obtained from the alternative circuit of Figure 5(b) which is logically equivalent with the circuit in Figure 3(b).

Finally, the layout of the functional cell can be optimized as shown in Figure 5(d) and the size of this array is almost one half that of the basic layout shown in Figure 3(d).



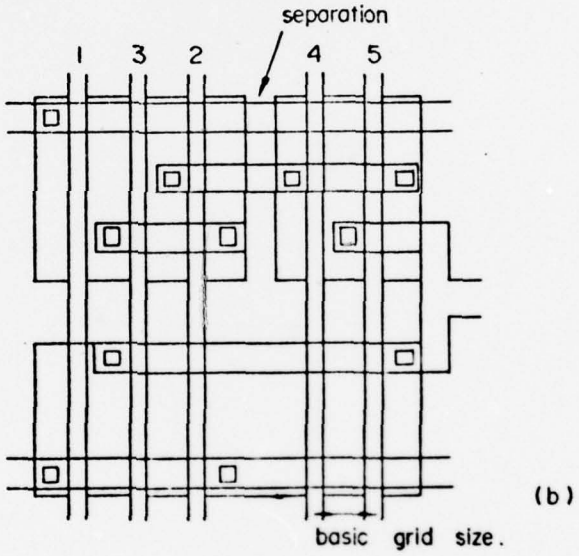


Figure 4: Optimization of layout.
a) simple transformation of Figure 3(c)
b) optimal arrangement for the circuit in Figure 3(b).

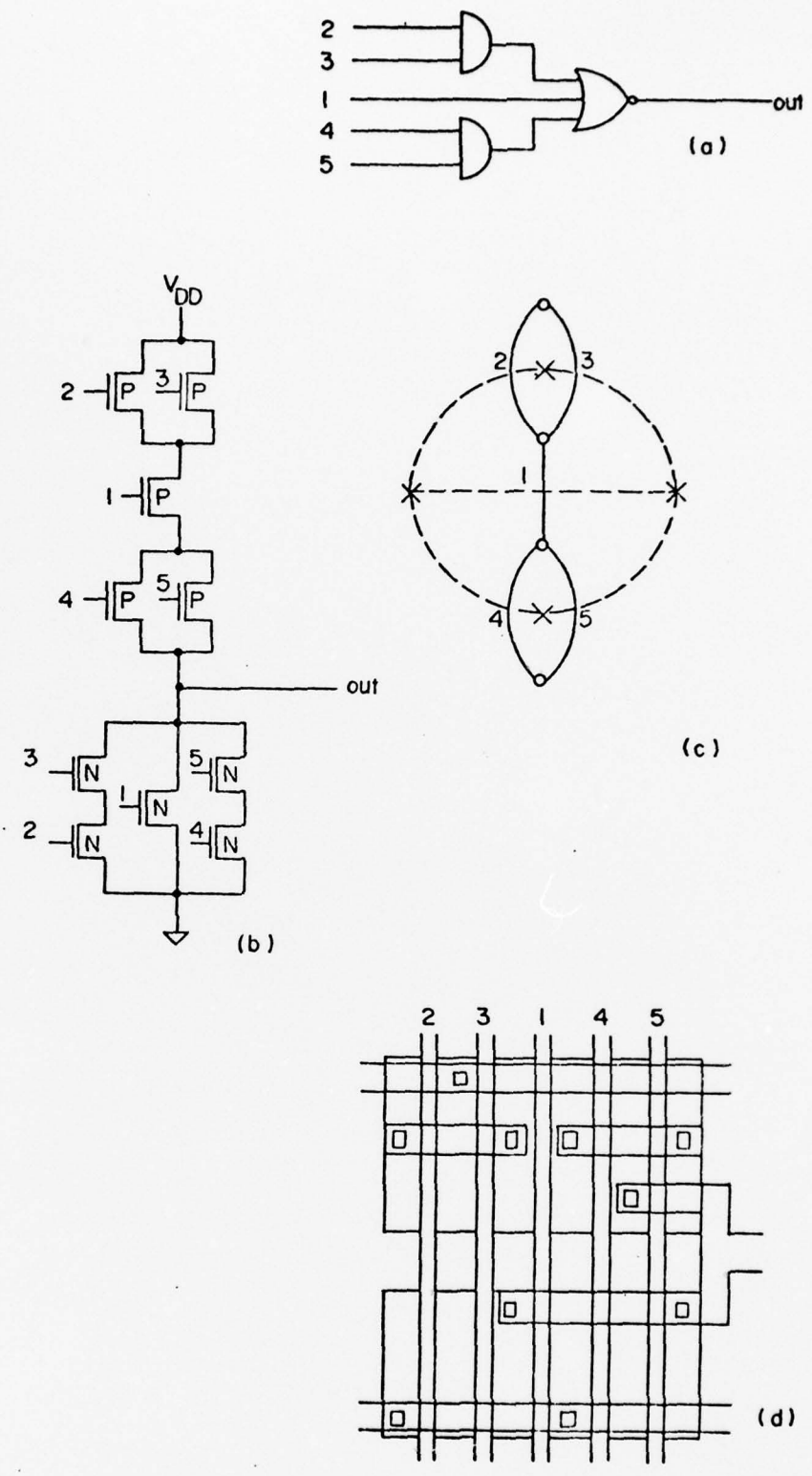


Figure 5: An alternative circuit and optimal layout.
a) logic diagram b) circuit c) graph model d) layout

In general, the area of a functional cell is calculated as follows: area = width * height

where: height = constant

width = basic grid size * (number of inputs + number of separations + 1)

A separation is required when there is no connection between physically adjacent transistors as illustrated in Figure 4(b). Since both the cell height and the basic grid size are a function of the technology employed, an optimal layout is obtained by minimizing the number of separations.

5.2 Graph-Theoretical Algorithm

Definition: An elementary series-parallel graph G(V,E,v,w) consists of a single edge e joining vertices v and w. Hence, its vertex set V = { v,w } and its edge set E = {(v,w)}. The vertices v and w are the termination points of G.

Definition: The series composition G(V,E,v,w) of two series-parallel graphs G'(V',E',v',w') and G"(V",E",v",w") is a new graph constructed from G' and G" as follows:

1) V = V' U V" U {u} - {w',v"} where u is a new vertex created to replace vertices w' and v" which are merged together.

2) E = E' U E" where every occurrence of w' and v" is replaced by u.

3) v = v' and w = w" are the termination points of the new graph

Definition: The parallel composition G(V,E,v,w) of two series-parallel graphs G'(V',E',v',w') and G"(V",E",v",w") is a new graph constructed from G' and G" as follows:

1) $V = V' \cup V'' \cup \{v,w\} - \{v',w',v'',w''\}$ where v and w are new vertices created to replace v',v" and w',w" respectively.

2) $E = E' \cup E''$, where ever occurrence of v' and v" is replaced by v and every occurrence of w' and w" is replaced by w.

3) The new termination points are $v = v' = v''$ and $w = w' = w''$.

Definition: An elementary series-parallel graph is a series-parallel graph.

A graph obtained by successive series and parallel *compositions* on a set of elementary series-parallel graphs is a series-parallel graph.

The graph model of a circuit is defined as follows. A p-side graph and a n-side graph are models of the p-MOS side and the n-MOS side of a circuit, respectively. The p-MOS side graph is defined as follows:

- every gate/drain potential is represented by a vertex.
- every transistor is represented by an edge, connecting the

vertices representing the source and drain.

The n-side graph can be defined in a similar way. An example of such a graph is shown in Figure 5.

Because of the restriction on the CMOS circuits under consideration, both the n-side and p-side graphs are series-parallel graphs.

Edges correspond to transistors in both graphs and they are connected in a series/parallel manner according to the series/parallel connections of transistors in the circuit. The names of input signals are used to label those edges. The p-side graph and the n-side graph are dual by the assumption of section 3 and each corresponding pair of edges has a common label.

The following property of the graph model is of interest for the optimal layout of CMOS circuits:

If two edges x and y are adjacent in the graph model, then it is possible to place the corresponding gates in a physically adjacent position of an array and hence, connect them by a diffusion area. In order to minimize the number of separation areas, it is necessary to find a set of minimum-size paths which correspond to chains of transistors in the array. As indicated in

section 5.1, such a set will result in a minimal area layout.

If there exists an Euler path in the graph model, then all gates can be chained by diffusion areas. If there is no Euler path then the graph can be decomposed into several subgraphs which have Euler paths. In the latter case, each Euler path corresponds to a chain of transistors that is separated from another such chain by a separation area.

In order to reduce the size of an array it is necessary to find a pair of paths on the dual graph models, with the same sequence of labels, because p-type and n-type gates corresponding to the same input signal have the same horizontal position in the CMOS array. For example, the path <1,3,2,4,5> of the n-side graph in Figure 3(c) produces a chain of gates on the n-MOS side as shown in Figure 4(b). There is, however, no corresponding Euler path in the p-side graph. Therefore, the gates on the p-MOS side are separated between gate 2 and gate 4 as shown in Figure 4(b).

On the other hand, path <2,3,1,4,5> is an Euler path in both the p-side and the n-side graph of Figure 5(c). Therefore, all gates can be chained together by diffusion areas without any separation areas as shown in Figure 5(d).

The general algorithm is shown below:

1) enumerate all possible decompositions of the graph model to find the minimum number of Euler paths that cover the graph.

2) chain the gates by means of a diffusion area according to the order of the edges in each Euler path.

3) if more than 2 Euler paths are necessary to cover the graph model, then provide a separation area between each pair of chains.

6. REDUCTION OF THE PROBLEM

In order to find the minimum number of Euler paths, it is possible to take advantage of the reduction method which is illustrated in Figure 6: an odd number of series or parallel edges can be reduced to a single edge.

Definition: The reduced graph is obtained by replacing an odd number of series (parallel) edges by a single edge, until no further reduction is possible.

Theorem 1: If there is an Euler path in the reduced graph, then there exists an Euler path in the original graph.

(Proof) It is possible to reconstruct an Euler path in the original graph by replacing each edge of the Euler path in the reduced graph by a sequence of the original odd number of edges.

Sometimes this reduction makes the problem trivial. For example, the graph model of Figure 8 is reduced to a single edge and the existence of an Euler path in the graph model is obvious.

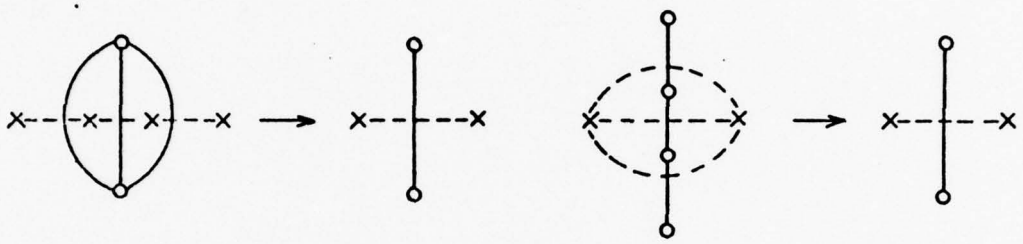


Figure 6: Reduction of odd number of edges.

Theorem 2: If the number of inputs to every AND/OR element is odd, then

1) the corresponding graph model has a single Euler path.
2) there exists a graph model such that the sequence of edges on an Euler path corresponds to the vertical order of inputs on a planar representation of the logic diagram.

(Proof) (1) The CMOS implementation of an AND/OR element has a number of series/parallel transistors that is equal to the number of inputs to that element (see section 4). Since the number of edges in series or in parallel is always odd, the graph model can be reduced to a single edge which is an Euler path itself. So there exists an Euler path on the original graph according to theorem 1.

(2) It is possible to construct the graph as follows (see the example in Figure 7(c)):

(a) Start with an edge corresponding to the circuit's output.
(b) Select an edge corresponding to the output of a gate and replace it by the series-parallel graph for that gate.

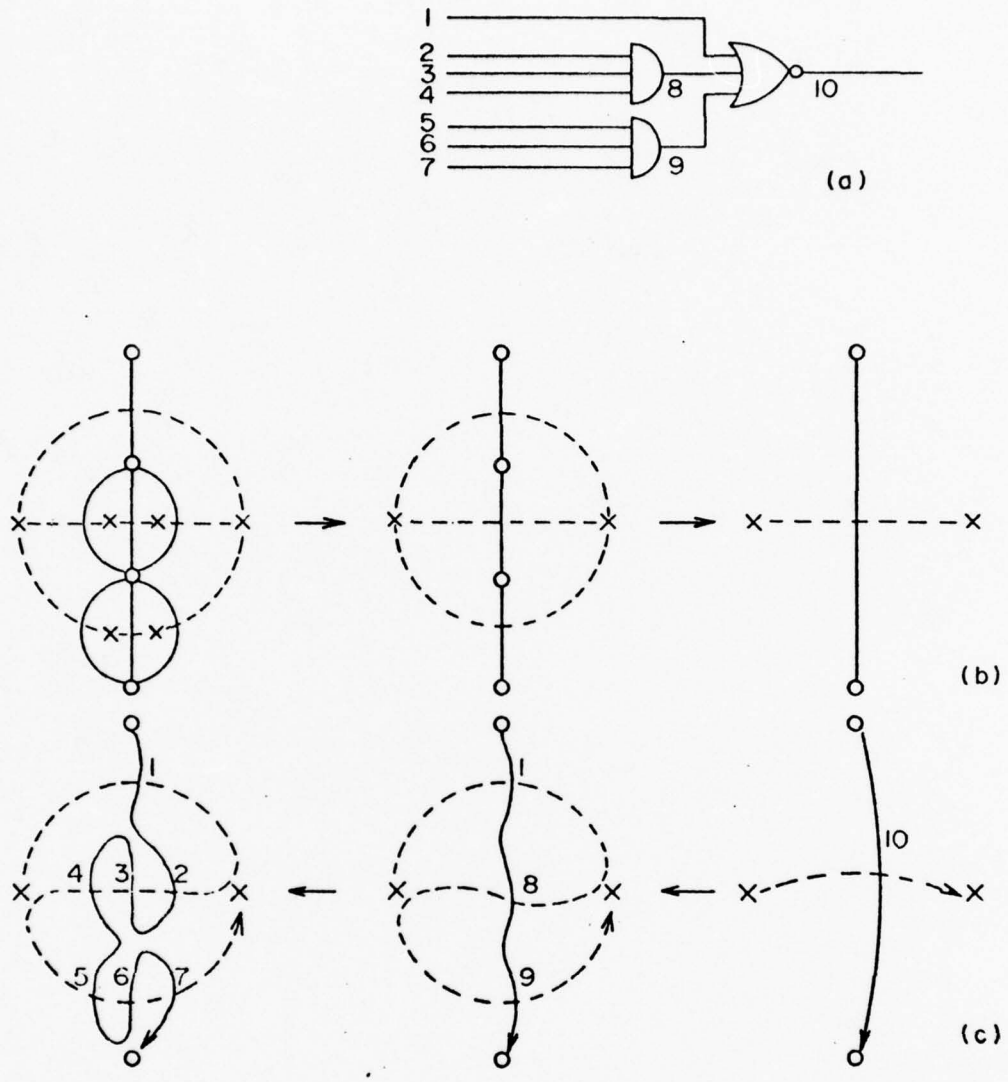


Figure 7: Application of reduction rule.
a) logic diagram b) graph model and its reduction.
c) reconstruction of an Euler path.

(c) Reorganize the sequence of new edges on the Euler path being constructed such that it corresponds to the vertical order of the inputs on the planar representation of the logic diagram. Such a rearrangement of edges in the Euler path is always possible when the number of inputs to an AND/OR element and hence the number of edges in series or in parallel is odd.

7. HEURISTIC ALGORITHM

Since the graph-theoretical algorithm of section 5 is exhaustive in nature, a heuristic algorithm which takes advantage of theorem 2 is proposed. Additional inputs called "pseudo"inputs are introduced and the original problem is modified so that every gate in a logic diagram has an odd number of inputs. It is guaranteed by theorem 2 that there exists an Euler path for this modified problem. This Euler path contains edges corresponding to the original inputs and also edges corresponding to the new "pseudo"inputs which are possible separation areas. The topology of the circuit should be selected such that the number of separation areas is minimized.

The heuristic algorithm consists of the following steps:

1) To every gate with an even number of inputs a "pseudo" input is added.

2) Add this new input to the gate in such a way that the planar representation of the logic diagram shows a minimal interlace of "pseudo" and real inputs. It should be noted that a "pseudo" input at the top or at the bottom of the logic diagram does not contribute to the separation areas, as illustrated in Figure 7(b) and Figure 7(c).

3) Construct the graph model such that the sequence of edges corresponds to the vertical order of inputs on the planar logic diagram.

4) Chain together the gates by means of diffusion areas, as indicated by the sequence of edges on the Euler path. "Pseudo " edges indicate separation areas.

5) The final circuit topology can be derived by deleting "pseudo" edges in parallel with other edges and by contracting "pseudo" edges in series with other edges.

The minimization of the separation areas can be performed on a logic diagram which nicely shows the structure of the series/ parallel graph.

Figure 8 shows the application of this heuristic algorithm to the problem of Figure 3. The same result as in Figure 5 is found easily. In general, new additional inputs correspond to separation areas, but in this case they do not actually separate the chain of gates because they are on both ends.

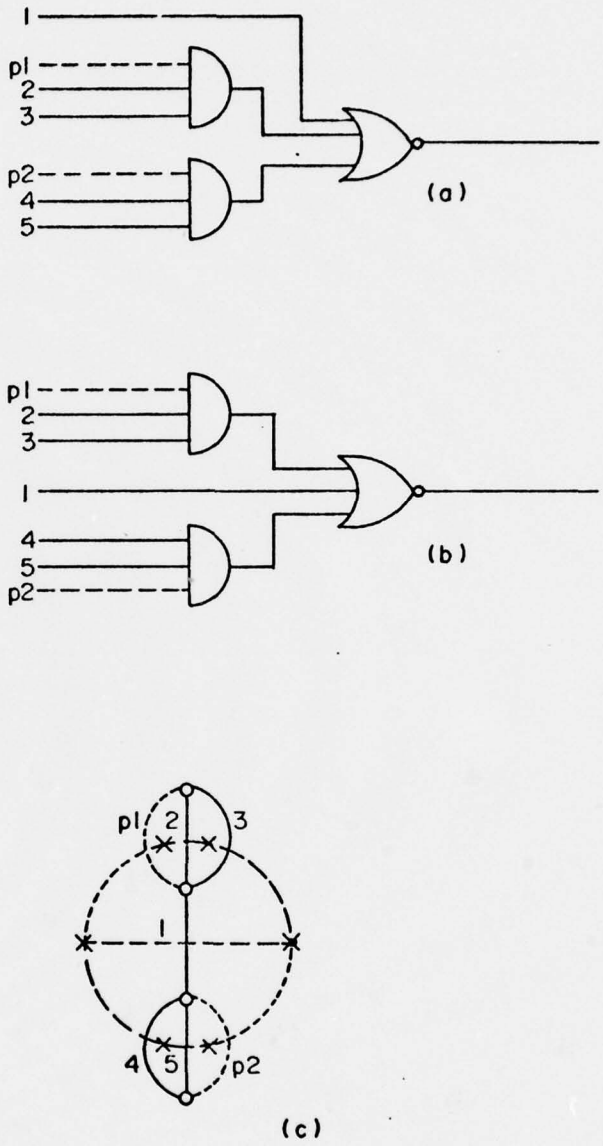


Figure 8: Application of the heuristic algorithm
a) new inputs p1 and p2 are added.
b) optimal sequence of inputs without the interlace of p1 or p2.
c) circuit with the dual path {p1,2,3,1,4,5,p1}

This heuristic algorithm does not necessarily give the optimal layout. However, if the resulting sequence has no separation areas, it is the real optimal solution.

Figure 9 is a four-bit carry look-ahead circuit from Hewlett-Packard's processor MC2 [5]. The circuit has no Euler path. But the alternative circuit in Figure 10(c) has an Euler path on the dual graphs. This optimal solution is found easily by the heuristic algorithm as shown in Figure 10. Figure 11 shows that the space for the functional cell is less than one third of the conventional gate realization.

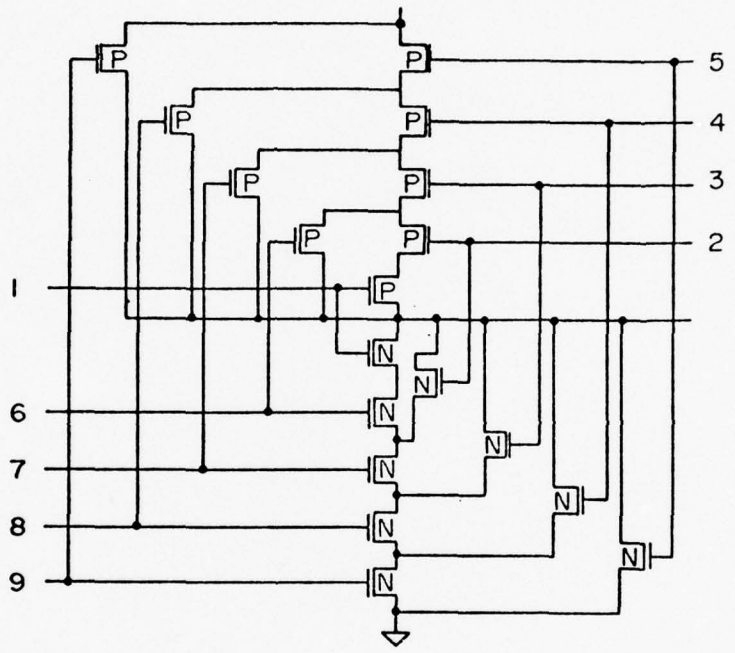


Figure 9: Carry look-ahead circuit
(From Hewlett-Packard Journal, April 1977)

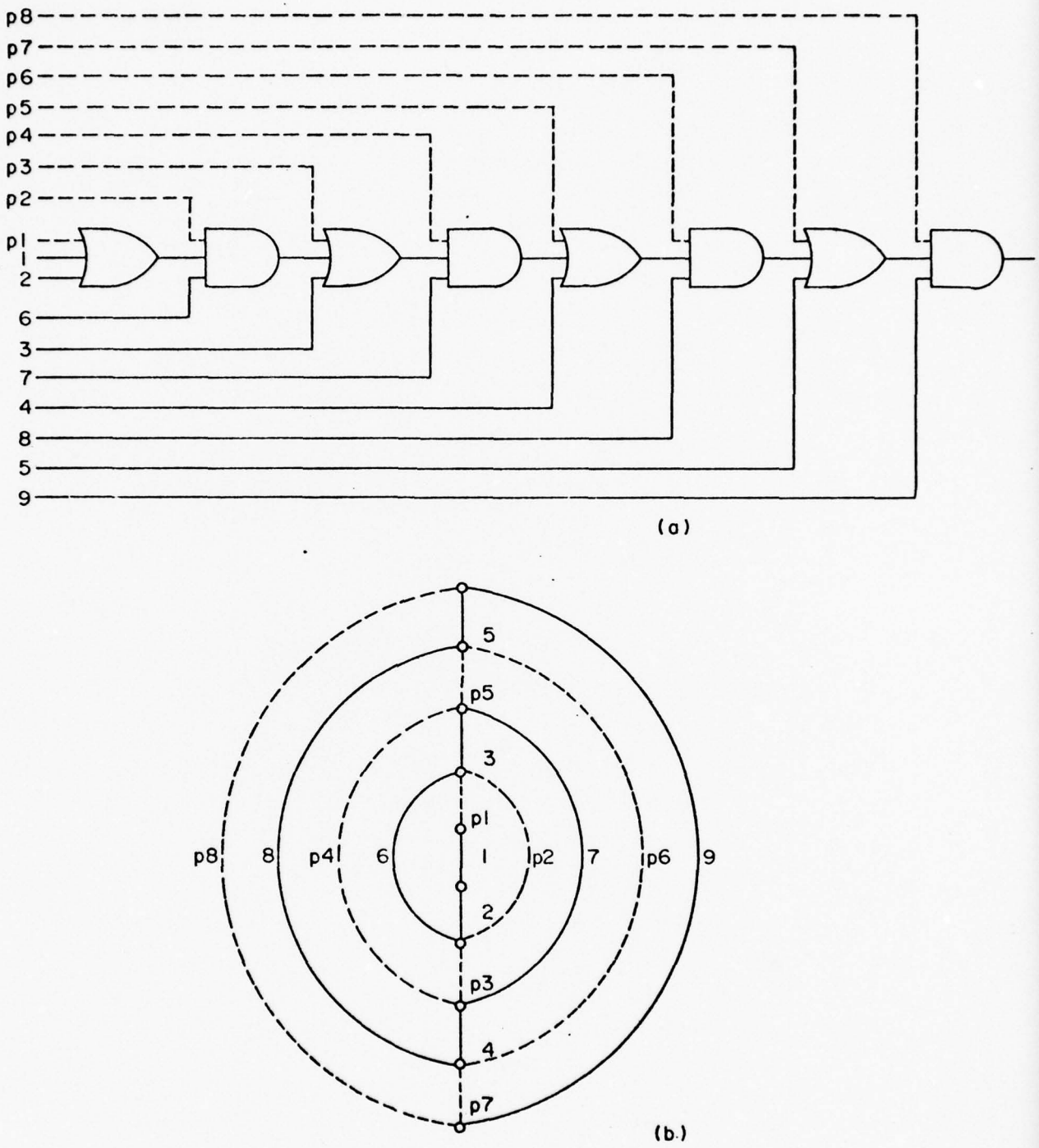


Figure 10: Alternative topology of the carry look-ahead circuit
a) the optimal sequence of variables
b) graph with an Euler path on the dual graphs

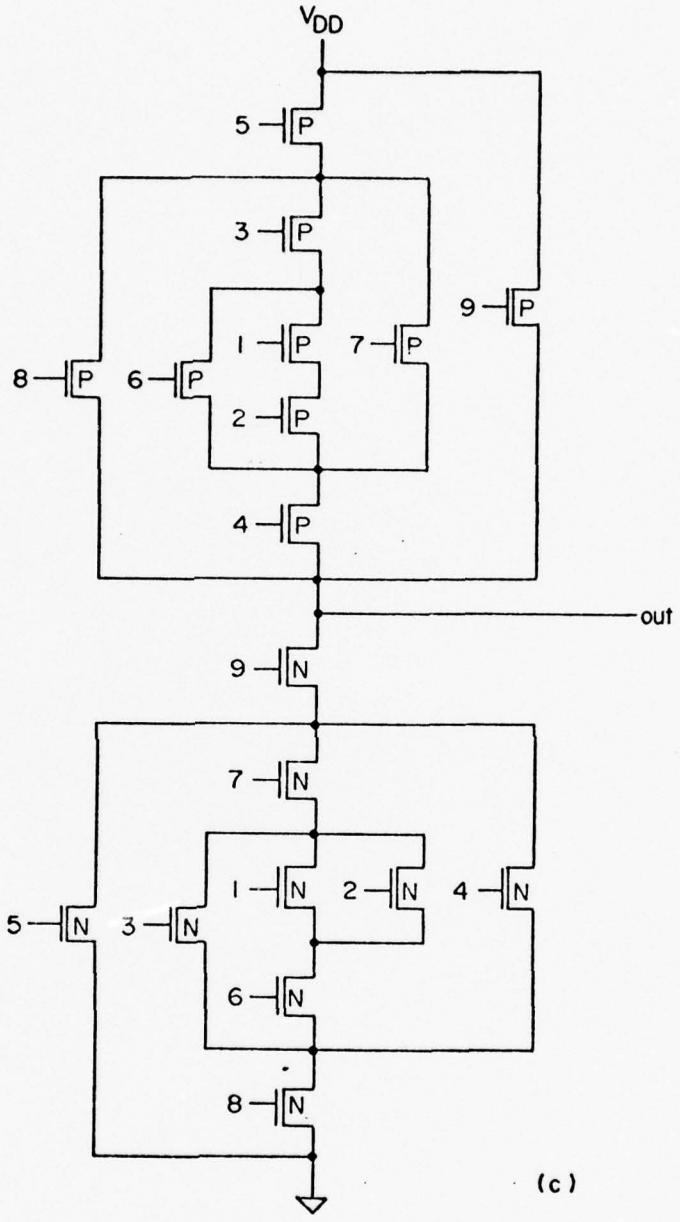
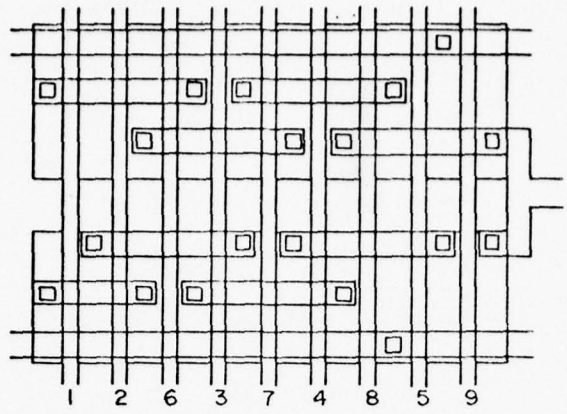


Figure 10: c) circuit diagram



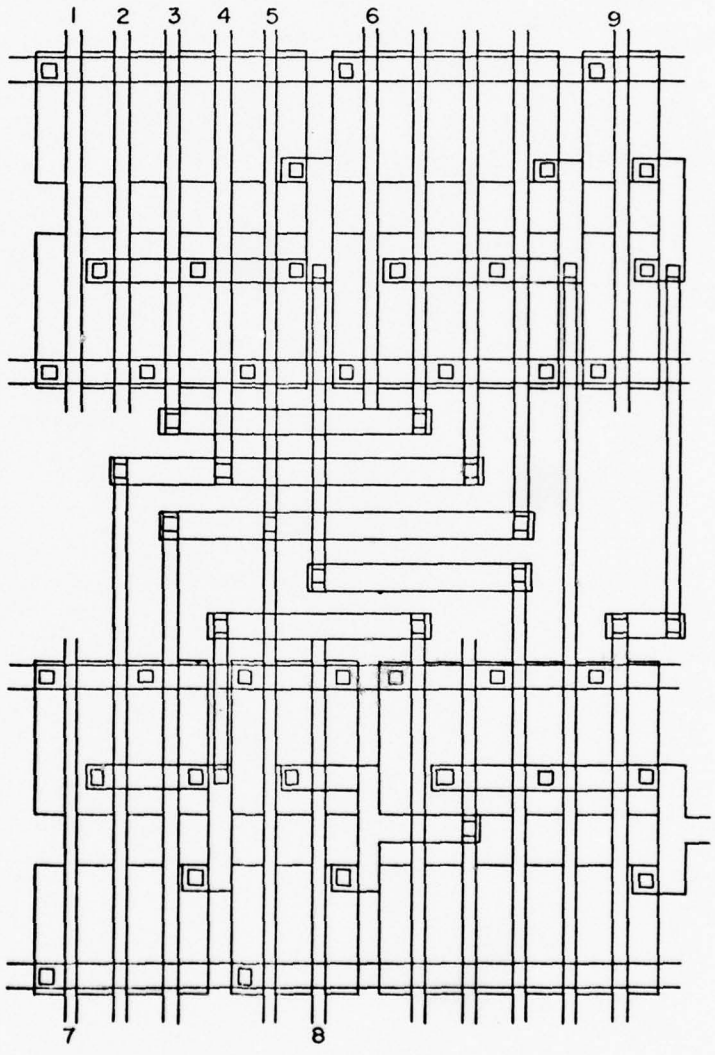


Figure 11: Comparison of space
a) functional cell realization
b) conventional NAND realization

8. CONCLUSIONS

A systematic survey of MOS functional cells and the enumeration of random logic functions made it clear that there are thousands of useful cells. A systematic method to implement a function on an array of CMOS transistors has been shown and a graph-theoretical algorithm which minimizes the size of the array has been presented An example showed that the functional cell approach can reduce the space of a conventional NAND gate realization considerably. In general, a significant space reduction can be expected.

The CMOS functional array is also useful as a basic cell for a conventional design automation system. Implementing functional arrays into a MOS LSI design automation system will be considered after further studies of logic synthesis and performance validation.

9. ACKNOWLEDGEMENTS

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APPENDIX

Enumeration of C-MOS Functional Cells.

A restriction to series/parallel connection and the duality between p-MOS side and n-MOS side are assumed. Logically equivalent circuits, for example, circuits in Figure 3(b) and in Figure 5(b) are counted only once.

Definitions:

T(m,n) is a set of cells which have m levels on the p-MOS side and n levels on the n-MOS side.

S(m,n) is a subset of T(m,n) such that the p-MOS side of a cell c of S(m,n) is a series connection of 2 components.

P(m,n) is the complement of S(m,n) with respect to T(m,n).

L(k) = { t|t is in T(m,n) and Max(m,n) = k}, that is, L(k) is a set of cells which have k levels.

Theorem 1: $|S(m,n)| = |P(n,m)|$ for (m,n) not equal to (1,1).

(Proof) Assume (m,n) not equal to (1,1). For any circuit c in P(m,n), the dual circuit of c is in S(n,m). For any circuit d in S(n,m), the dual circuit of d is in P(m,n). So there is one to one mapping between P(m,n) and S(n,m).

Lemma 1:

$$|L(k)| = 2[\sum_{i=1}^{k-1} \{|S(i,k)| + |S(k,i)|\} + |S(k,k)|].$$

Definition: C1 - C2 - ... - Ci is a cell such that the p-MOS part of the cell is a series connection of p-MOS parts in cells C1, C2, ... and Ci.

Hence, P(m1,n1) - P(m2,n2) - ... - P(mi,ni) =
{C1 - C2 - ... - Ci|Ci is in P(m1,n1), C2 is in P(m2,n2), ..., ci is in P(mi,ni)}.

Theorem 2: P(m1,n1) - P(m2,n2) - ... - P(mi,ni) is a subset of S(m,n), where m = m1 + m2 + ... + mi, and n = Max(n1, n2, ... , ni).

(Proof) The longest path on the p-MOS side is m1 + m2 ... + mi by definition. The longest path on the n-MOS side is Max(n1, n2, ..., ni) because it is equal to the maximal cutset on the p-MOS side.

L(k) can be decomposed using theorem 2 and enumerated using theorem 1 and lemma 1 as follows:

L(1) is the union of the following two sets:

$S(1,1) = \not\emptyset$,

P(1,1) = {inverter}.

So |L(1)| = 1.

L(2) is the union of the following sets:

$S(1,2) = \not\emptyset$,

S(2,1) = { P(1,1) - P(1,1) },

S(2,2) = { P(1,1) - P(1,2),

P(1,2) - P(1,2) },

and their dual forms.

So |L(2)| = 6.

L(3) is the union of the following sets:

$S(1,3) = \not\emptyset$

S(3,1) = { P(1,1) - P(1,1) - P(1,1) }

S(2,3) = { P(1,1) - P(1,3),

$$P(1,2) - P(1,3),$$

$$P(1,3) - P(1,3) \}$$

$$S(3,2) = \{ P(1,1) - P(1,1) - P(1,2),$$

$$P(1,1) - P(1,2) - P(1,2),$$

$$P(1,2) - P(1,2) - P(1,2),$$

$$P(1,1) - P(2,2),$$

$$P(1,2) - P(2,2) \}$$

$$S(3,3) = \{ P(1,1) - P(1,1) - P(1,3),$$

$$P(1,1) - P(1,2) - P(1,3),$$

$$P(1,2) - P(1,2) - P(1,3),$$

$$P(1,1) - P(1,3) - P(1,3),$$

$$P(1,2) - P(1,3) - P(1,3),$$

$$P(1,3) - P(1,3) - P(1,3),$$

$$P(1,1) - P(2,3),$$

$$P(1,2) - P(2,3),$$

$$P(1,3) - P(2,2),$$

$$P(1,3) - P(2,3) \}$$

and their dual forms

So $|L(3)| = 80$.

By a similar enumeration one can derive that

$$|L(4)| = 3434.$$

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Designers of MOS LSI circuits can take advantage of complex functional cells in order to achieve better performances. This paper discusses the implementation of a random logic function on an array of CMOS transistors. A graph-theoretical algorithm which minimizes the size of an array is presented. This method is useful for the design of cells used in conventional design automation sytems.

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